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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/667,394	ANG, LIN PING	
	Examiner	Art Unit	
	Paul Saunders	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) *62 and 68* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. **Figures 1, 2, 3** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

1. Claim 15 objected to because of the following informalities. Appropriate correction is required.

Regarding **claim 15**, antecedent basis for "said *M* sample and hold circuits" not found. It is suggested to change the italicized to "Y".

Regarding **claim 16**, the following is not clear: "pixels are being read and *the another* operating mode." It is suggested to change the italicized to "another".

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 62, 68** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims are inconsistent with the specification disclosure. The specification disclosure teaches the storage device storing one pixel signal from either of two columns during each reading of a row. The claim requires the storage device to store two pixel signals from two adjacent columns on the same row during each reading of an even row. Claims 62, 68 raise an unreasonable degree of uncertainty in light of the specification disclosure and are therefore withdrawn from consideration.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-6,10-16,29-35,39-44,57-60,63-66** rejected under 35 U.S.C. 102(e) as being anticipated by

a. *Nam* (US 2004/0135910 A1).

Regarding **claim 1**, *Nam* discloses an imager device comprising:

a plurality of pixels arranged in at least a first and second column, each column

having a column line to which pixels in the column can be connected; first 638-6381 and second 637-6371 sample and hold circuits for sampling and holding signals output from the pixels on said column lines (fig. 6);

a multiplexer coupling at least first and second column lines with said first and second sample and hold circuits and being operable, in a first mode, to respectively couple said first and second sample and hold circuits to said first and second column lines and being operable, in a second mode, to respectively couple said first and second sample and hold circuits to said second and first column lines (Abstract, fig. 6, [0023]).

Regarding **claim 2**, *Nam* further discloses the imager device of claim 1, wherein the plurality of pixels comprises an array of complementary metal oxide semiconductor pixels (fig. 6, [0024, 0052]).

Refer to the rejection of the parent claim(s).

Regarding **claim 3**, *Nam* further discloses the imager device of claim 1, wherein said multiplexer is controlled such that signals associated with a first pixel type are sampled and held by said first sample and hold circuit and signals of a pixel type different than the first pixel type are sampled and held by said second sample and hold circuit (fig. 6, [0054, 0055]).

Refer to the rejection of the parent claim(s).

Regarding **claim 4**, *Nam* further discloses the imager device of claim 3, wherein the first pixel type is a first pixel color and the pixel type other than the first pixel type is at least a second pixel color (fig. 6, 7, [0054-0056]).

Refer to the rejection of the parent claim(s).

Regarding **claim 5**, *Nam* further discloses the imager device of claim 3, wherein the first pixel type is a first pixel color and the pixel type other than the first pixel type comprises second and third pixel colors (fig. 6, 7, [0054-0056]).

Refer to the rejection of the parent claim(s).

Regarding **claim 6**, *Nam* further discloses the imager device of claim 1 further comprising a column decoder 610 connected to and supplying control signals to said sample and hold circuits, said column decoder controlling said sample and hold circuits such that signals associated with a first pixel type are output on a first output channel and signals of a pixel type different than the first pixel type are output on a second output channel (fig. 6, 7, 9, [0054-0056, 0060-0066] – 610 is a column decoder from a sideways point of view supplying control signals (PhiSEven, PhiSOdd) to the sample and hold circuits such that the first and second pixel types are not output on the same channel).

Refer to the rejection of the parent claim(s).

Regarding **claim 10**, *Nam* further discloses the imager device of claim 1, wherein said multiplexer comprises a plurality of switching circuits 634-636 (fig. 6, [0053]).

Refer to the rejection of the parent claim(s).

Regarding **claim 11**, *Nam* further discloses the imager device of claim 10, wherein said switching circuits reside between the pixels and sample and hold circuits (fig. 6).

Refer to the rejection of the parent claim(s).

Regarding **claim 12**, *Nam* further discloses the imager device of claim 10, wherein said switching circuits reside in an input portion of the sample and hold circuits (fig. 9A, [0061]).

Refer to the rejection of the parent claim(s).

Regarding **claim 13**, *Nam* further discloses the imager device of claim 10, wherein said switching circuits comprise one switching configuration when a row being read is an even numbered row and a second switching configuration when a row being read is an odd numbered row (Abstract, [0023]).

Refer to the rejection of the parent claim(s).

Regarding **claim 14**, *Nam* further discloses an image device comprising: a plurality of pixel signals arranged in N columns, each column having a respective column line to which the pixels in the column can be connected (fig. 6, [0054]); a plurality Y of sample and hold circuits 637-6371, 638-6381, for sampling and holding signals output from said pixels; and a multiplexing circuit for coupling, in one operating mode, one of said N column lines to one of said sample and hold circuits and, in another operating mode, coupling a different one of said N columns to said one sample and hold circuit (fig. 6, [0056, 0058]).

Regarding **claim 15**, *Nam* further discloses the imager device of claim 14, wherein each of said Y sample and hold circuits comprise respective output lines (fig. 6 – the output lines between 637,638 and 632, 630 respectively).

Refer to the rejection of the parent claim(s).

Regarding **claim 16**, *Nam* further discloses the imager device of claim 14, wherein the first operating mode is a readout operation in which even numbered rows of pixels are being read and the another operating mode is a readout operation in which odd numbered rows of pixels are being read (Abstract, [0023]).

Refer to the rejection of the parent claim(s).

Regarding **claim 29**, *Nam* discloses a processor system comprising:

an imager device comprising: an array of pixels arranged in a plurality of rows and columns; a plurality of first sample and hold circuits 638-6381, each first sample and hold circuit being connected to a respective even numbered column of said array; a plurality of second sample and hold circuits 637-6371, each second sample and hold circuit being connected to a respective odd numbered column of said array (fig. 6); and

a multiplexer comprising a plurality of switching circuits 633, 634, 635, 636, each switching circuit being associated with and connected to a respective first sample and hold circuit and its associated even numbered column and a respective second sample and hold circuit and its associated odd numbered column, wherein said switching circuits are controlled such that signals associated with a first pixel type are sampled and held by said first sample and hold circuits and signals of a pixel type different than the first pixel type are sampled and held by said second sample and hold circuits (fig. 6, [0056, 0058] – switching circuits being controlled by even and odd signals such that green signals will always be sampled by the first sample and hold circuit).

Regarding **claim 30**, *Nam* further discloses the system of claim 29, wherein the array of pixels comprises an array of complementary metal oxide semiconductor pixels.

Refer to the rejection of the parent claim(s) and claim 2.

Regarding **claim 31**, *Nam* further discloses the system of claim 29, wherein the pixels of the first pixel type reside in even numbered and odd numbered columns (fig. 6 - green being the first type of pixels).

Refer to the rejection of the parent claim(s).

Regarding **claim 32**, *Nam* further discloses the system of claim 31, wherein the pixels of the pixel type other than the first pixel type reside in even numbered and odd numbered columns (fig. 6 – red and blue being the other type of pixels).

Refer to the rejection of the parent claim(s).

Regarding **claim 33**, *Nam* further discloses the system of claim 29, wherein the first pixel type is a first pixel color and the pixel type other than the first pixel type is at least a second pixel color (fig. 6).

Refer to the rejection of the parent claim(s).

Regarding **claim 34**, *Nam* further discloses the system of claim 29, wherein the first pixel type is a first pixel color and the pixel type other than the first pixel type comprises second and third pixel colors (fig. 6).

Refer to the rejection of the parent claim(s).

Regarding **claim 35**, *Nam* further discloses the system of claim 29 further comprising a column decoder connected to and supplying control signals to said sample and hold circuits, said column decoder controlling said sample and hold circuits such that signals associated with the first pixel type are output on a first output channel and signals of a pixel type different than the first pixel type are output on a second output channel.

Refer to the rejection of the parent claim(s) and claim 6.

Regarding **claim 39**, *Nam* further discloses the system of claim 29, wherein said switching circuits reside between the array and sample and hold circuits.

Refer to the rejection of the parent claim(s) and claim 11.

Regarding **claim 40**, *Nam* further discloses the system of claim 29, wherein said switching circuits reside in an input portion of the sample and hold circuits.

Refer to the rejection of the parent claim(s) and claim 12.

Regarding **claim 41**, *Nam* further discloses the system of claim 29, wherein said switching circuits comprise one switching configuration when a row being read is an even numbered row and a second switching configuration when a row being read is an odd numbered row (fig. 7, [0054-0055]).

Refer to the rejection of the parent claim(s).

Regarding **claim 42**, *Nam* further discloses the system of claim 29, wherein each switching circuit comprises: a first input switch coupled between a pixel line from the even numbered column and a first charge storage device; a second input switch coupled between the connection of the first input switch and a third input switch; said third input switch being coupled between the connection of the third input switch and a fourth input switch; and said fourth input switch being coupled between a pixel line from the odd numbered column and a second charge storage device.

Refer to the rejection of the parent claim(s) and claim 26.

Regarding **claim 43**, *Nam* further discloses the system of claim 42, wherein said first and fourth switches are closed when a row being read is an even numbered row.

Refer to the rejection of the parent claim(s) and claim 27.

Regarding **claim 44**, *Nam* further discloses the system of claim 42, wherein said second and third switches are closed when a row being read is an odd numbered row.

Refer to the rejection of the parent claim(s) and claim 28.

Regarding **claim 57**, *Nam* discloses a processor system comprising: an imager device, said imager device comprising:

a plurality of pixel signals arranged in N columns (fig. 10), each column having a respective column line to which the pixels in the column can be connected (Abstract);

a plurality Y of sample and hold circuits 1038-10381, 1037-10371 for sampling and holding signals output from said pixels; and

a multiplexing circuit 1040-10401, 1042-10421 for coupling, in one operating mode, one of said N column lines to one of said sample and hold circuits and, in another operating mode, coupling a different one of said N columns to said one sample and hold circuit (fig. 10, [0067]).

Regarding **claim 58**, *Nam* discloses a method of operating an imager device, said method comprising the steps of:

storing signals associated with a first pixel type in a first storage device 638 associated with a first column of pixels (fig. 6 – column having pixels 640, 650);

storing signals associated with a type other than the first pixel type in a second storage device 637 associated with a second column of pixels (fig. 6 – column having pixels 645, 655);

outputting the signals from the first storage device to a first channel (fig. 6 – connection between 638 and 630); and outputting the signals from the second storage device to a second channel (fig. 6 – connection between 637 and 632).

Regarding **claim 59**, *Nam* further discloses the method of claim 58 wherein said step of storing signals associated with the first pixel type comprises: determining whether a row being read is even (fig. 7); and if it is determined that the row is even, storing a signal received from a first column in the first storage device (fig. 7, [0054-0056] – when an even row is read the first pixel type from the first column is stored in the first storage).

Refer to the rejection of the parent claim(s).

Regarding **claim 60**, *Nam* further discloses the method of claim 59, wherein said step of storing signals associated with the first pixel type further comprises: connecting the first storage device to a second column if it is determined that the row is odd (fig. 7); and storing a signal received from the second column in the first storage device (fig. 7, [0054-0056] – when an odd row is read the first pixel type from the second column is stored in the first storage).

Refer to the rejection of the parent claim(s).

Regarding **claim 63**, *Nam* discloses a method of operating a CMOS color imager device, said method comprising the steps of:

storing signals associated with green pixels 645, 650 in a first storage device 638 associated with a first column of pixels (fig. 6 – column having pixels 640, 650); and

storing signals associated with red and blue pixels 640, 655 in a second storage device 637 associated with a second column of pixels (fig. 6 – column having pixels 645, 655).

Regarding **claim 64**, *Nam* further discloses the method of claim 63 further comprising the steps of: outputting the signals from the first storage device to a first channel (fig. 6 – connection between 638 and 630); and outputting the signals from the second storage device to a second channel (fig. 6 – connection between 637 and 632).

Refer to the rejection of the parent claim(s).

Regarding **claim 65**, *Nam* further discloses the method of claim 63, wherein said step of storing signals associated with green pixels comprises: determining whether a row being read is even; and if it is determined that the row is even, storing a signal received from a first column in the first storage device (Abstract, fig. 6, 7 – the second row first column contains pixel 650 which is green and will be stored in 638).

Refer to the rejection of the parent claim(s).

Regarding **claim 66**, *Nam* further discloses the method of claim 65, wherein said step of storing signals associated with the green pixels further comprises: connecting the first storage device to a second column if it is

determined that the row is odd; and storing a signal received from the second column in the first storage device (Abstract, fig. 6, 7 – the first row second column contains pixel 645 which is green and will be stored in 638).

Refer to the rejection of the parent claim(s).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 7-9,36-38** rejected under 35 U.S.C. 103(a) as being unpatentable over

a. *Nam* (US 2004/0135910 A1)

in view of

b. *Fossum* (US 5,471,515 A, *Fossum* et al.).

Regarding **claim 7**, *Nam* does not disclose the imager device of claim 6, wherein the first output channel comprises two output lines and the second output channel comprises two output lines.

Fossum discloses a sample and hold circuit with an output channel having two (V OUT S, V OUT R) output lines (fig. 3, col. 3 line 21-col. 4 line 3). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the previous sample and hold circuit (*Nam* fig. 6, 9A) to receive a signal from an even or odd column but to separately store and output

the signal and reset voltages wherein the previous amplifier following the sample and hold circuit would also take the difference of the two output signals as taught above by *Fossum* because it is functionally equivalent.

Refer to the rejection of the parent claim(s).

Regarding **claim 8**, *Nam* in view of *Fossum* discloses the imager device of claim 7, wherein said first sample and hold circuit samples and holds reset and pixel signals associated with the first pixel type, the pixel signals being output on one output line of the first output channel and the reset signals being output on a second output line of the first output channel.

Refer to the rejection of the parent claim(s).

Regarding **claim 9**, *Nam* in view of *Fossum* discloses the imager device of claim 7, wherein said second sample and hold circuit samples and holds reset and pixel signals associated with the pixel type that is different than the first pixel type, the pixel signals being output on one output line of the second output channel and the reset signals being output on a second output line of the second output channel.

Refer to the rejection of the parent claim(s).

Regarding **claim 36**, *Nam* in view of *Fossum* discloses the system of claim 35, wherein the first output channel comprises two output lines and the second output channel comprises two output lines.

Refer to the rejection of the parent claim(s) and claim 7.

Regarding **claim 37**, *Nam* in view of *Fossum* discloses the system of claim 36, wherein said first sample and hold circuits sample and hold reset and pixel signals associated with the first pixel type, the pixel signals being output on one output line of the first output channel and the reset signals being output on a second output line of the first output channel.

Refer to the rejection of the parent claim(s) and claim 7.

Regarding **claim 38**, *Nam* in view of *Fossum* discloses the system of claim 36, wherein said second sample and hold circuits sample and hold reset and pixel signals associated with the pixel type that is different than the first pixels type, the pixel signals being output on one output line of the second output channel and the reset signals being output on a second output line of the second output channel.

Refer to the rejection of the parent claim(s) and claim 7.

4. **Claims 17-19,23-28,45-47,51-56** rejected under 35 U.S.C. 103(a) as being unpatentable over

c. *Nam* (US 2004/0135910 A1)

in view of

d. *Decker* (US 6,512,546 B1, *Decker* et al.).

Regarding **claim 17**, *Nam* discloses an imager device comprising:

an array of pixels arranged in a plurality of rows and columns, each even numbered row having alternating green 645 and red 640 pixels (fig. 6 – red and green are alternating in the beginning row), each odd numbered row having alternating blue 655 and green 650 pixels (fig. 6 – green and blue are alternating in the row following the beginning row);

a plurality of first sample and hold circuits 638-6381, each first sample and hold circuit being connected to a respective even numbered column of said array; a plurality of second sample and hold circuits 637-6371, each second sample and hold circuit being connected to a respective odd numbered column of said array (fig. 6 – each first and second sample and hold circuit are connected to an even and odd column); and

a plurality of switching circuits 633, 634, 635, 636, each switching circuit being associated with and connected to a respective first sample and hold circuit and its associated even numbered column and a respective second sample and hold circuit and its associated odd numbered column, wherein said switching circuits being controlled such that signals associated with green pixels are sampled and held by said first sample and hold circuits and signals associated with the red and blue pixels are sampled and held by said second sample and hold circuits

(fig. 6, [0056, 0058] – switching circuits being controlled by even and odd signals such that green signals will always be sampled by the first sample and hold circuit).

Nam does not expressly disclose a pattern in which the even numbered rows start with the first row and the odd rows start with the second row.

Decker discloses the even numbered rows starting with the first row and the odd numbered rows starting with the second row (fig. 3, col. 5 lines 25-35). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to begin numbering the first row starting with zero because it is functionally equivalent.

Regarding **claim 18**, *Nam* further discloses the imager device of claim 17, wherein the array of pixels comprises an array of complementary metal oxide semiconductor pixels (fig. 6, [0024, 0052]).

Refer to the rejection of the parent claim(s).

Regarding **claim 19**, *Nam* further discloses the imager device of claim 17, further comprising a column decoder connected to and supplying control signals to said sample and hold circuits, said column decoder controlling said sample and hold circuits such that signals associated with the green pixels are output on a first output channel and signals associated with the red and blue pixels are output on a second output channel.

Refer to the rejection of the parent claim(s) and claim 6.

Regarding **claim 23**, *Nam* further discloses the imager device of claim 17, wherein said switching circuits reside between the array and sample and hold circuits (fig. 6).

Refer to the rejection of the parent claim(s).

Regarding **claim 24**, *Nam* further discloses the imager device of claim 17, wherein said switching circuits reside in an input portion of the sample and hold circuits (fig. 9A, [0061]).

Refer to the rejection of the parent claim(s).

Regarding **claim 25**, *Nam* further discloses the imager device of claim 17, wherein said switching circuits comprise one switching configuration when a row being read is an even numbered row and a second switching configuration when a row being read is an odd numbered row (Abstract, [0023]).

Refer to the rejection of the parent claim(s).

Regarding **claim 26**, *Nam* further discloses the imager device of claim 17, wherein each switching circuit comprises: a first input switch coupled between a pixel line from the even numbered column and a first charge storage device; a second input switch coupled between the connection of the first input switch and

a third input switch; said third input switch being coupled between the connection of the third input switch and a fourth input switch; and said fourth input switch being coupled between a pixel line from the odd numbered column and a second charge storage device (fig. 6, [0054, 0055]).

Refer to the rejection of the parent claim(s).

Regarding **claim 27**, *Nam* further discloses the imager device of claim 26, wherein said first and fourth switches are closed when a row being read is an even numbered row (fig. 6, [0054, 0055]).

Refer to the rejection of the parent claim(s).

Regarding **claim 28**, *Nam* further discloses the imager device of claim 26, wherein said second and third switches are closed when a row being read is an odd numbered row (fig. 6, [0054, 0055]).

Refer to the rejection of the parent claim(s).

Regarding **claim 45**, *Nam* discloses a processor system comprising:

an imager device, comprising: an array of pixels arranged in a plurality of rows and columns, each even numbered row having alternating green and red pixels (fig. 6 – red and green are alternating in the beginning row), each odd numbered row having alternating blue and green pixels (fig. 6 – green and blue are alternating in the row following the beginning row);

a plurality of first sample and hold circuits 638-6381, each first sample and hold circuit being connected to a respective even numbered column of said array; a plurality of second sample and hold circuits 637-6371, each second sample and hold circuit being connected to a respective odd numbered column of said array (fig. 6 – each first and second sample and hold circuit are connected to an even and odd column); and

a plurality of switching circuits 633, 634, 635, 636, each switching circuit being associated with and connected to a respective first sample and hold circuit and its associated even numbered column and a respective second sample and hold circuit and its associated odd numbered column, wherein said switching circuits being controlled such that signals associated with green pixels are sampled and held by said first sample and hold circuits and signals associated with the red and blue pixels are sampled and held by said second sample and hold circuits (fig. 6, [0056, 0058] – switching circuits being controlled by even and odd signals such that green signals will always be sampled by the first sample and hold circuit).

Nam does not expressly disclose a pattern in which the even numbered rows start with the first row and the odd rows start with the second row.

Decker discloses the even numbered rows starting with the first row and the odd numbered rows starting with the second row (fig. 3, col. 5 lines 25-35). Therefore it would have been obvious to one of ordinary skill in the art at the time

of the invention to begin numbering the first row starting with zero because it is functionally equivalent.

Regarding **claim 46**, *Nam* further discloses the system of claim 45, wherein the array of pixels comprises an array of complementary metal oxide semiconductor pixels.

Refer to the rejection of the parent claim(s) and claim 2.

Regarding **claim 47**, *Nam* further discloses the system of claim 45, further comprising a column decoder connected to and supplying control signals to said sample and hold circuits, said column decoder controlling said sample and hold circuits such that signals associated with the green pixels are output on a first output channel and signals associated with the red and blue pixels are output on a second output channel.

Refer to the rejection of the parent claim(s) and claim 6.

Regarding **claim 51**, *Nam* further discloses the system of claim 45, wherein said switching circuits reside between the array and sample and hold circuits.

Refer to the rejection of the parent claim(s) and claim 11.

Regarding **claim 52**, *Nam* further discloses the system of claim 45, wherein said switching circuits reside in an input portion of the sample and hold circuits.

Refer to the rejection of the parent claim(s) and claim 12.

Regarding **claim 53**, *Nam* further discloses the system of claim 45, wherein said switching circuits comprise one switching configuration when a row being read is an even numbered row and a second switching configuration when a row being read is an odd numbered row.

Refer to the rejection of the parent claim(s) and claim 41.

Regarding **claim 54**, *Nam* further discloses the system of claim 45, wherein each switching circuit comprises: a first input switch coupled between a pixel line from the even numbered column and a first charge storage device; a second input switch coupled between the connection of the first input switch and a third input switch; said third input switch being coupled between the connection of the third input switch and a fourth input switch; and said fourth input switch being coupled between a pixel line from the odd numbered column and a second charge storage device.

Refer to the rejection of the parent claim(s) and claim 26.

Regarding **claim 55**, *Nam* further discloses the system of claim 54, wherein said first and fourth switches are closed when a row being read is an even numbered row.

Refer to the rejection of the parent claim(s) and claim 27.

Regarding **claim 56**, *Nam* further discloses the system of claim 54, wherein said first and fourth switches are closed when a row being read is an even numbered row.

Refer to the rejection of the parent claim(s) and claim 28.

6. **Claims 20-22,48-50** rejected under 35 U.S.C. 103(a) as being unpatentable over

b. *Nam* (US 2004/0135910 A1),

c. *Decker* (US 6,512,546 B1, *Decker* et al.)

as applied to claim 17 above, and further in view of

d. *Fossum* (US 5,471,515 A, *Fossum* et al.).

Regarding **claim 20**, *Nam* in view of *Decker* in further view of *Fossum* discloses the imager device of claim 19, wherein the first output channel comprises two output lines and the second output channel comprises two output lines.

Refer to the rejection of the parent claim(s) and claim 7.

Regarding **claim 21**, *Nam* in view of *Decker* in further view of *Fossum* discloses the imager device of claim 20, wherein said first sample and hold circuits sample and hold reset and pixel signals associated with the green pixels, the pixel signals being output on one output line of the first output channel and the reset signals being output on a second output line of the first output channel.

Refer to the rejection of the parent claim(s) and claim 7.

Regarding **claim 22**, *Nam* in view of *Decker* in further view of *Fossum* discloses the imager device of claim 20, wherein said second sample and hold circuits sample and hold reset and pixel signals associated with the red and blue pixels, the pixel signals being output on one output line of the second output channel and the reset signals being output on a second output line of the second output channel.

Refer to the rejection of the parent claim(s) and claim 7.

Regarding **claim 48**, *Nam* in view of *Decker* in further view of *Fossum* discloses the system of claim 47, wherein the first output channel comprises two output lines and the second output channel comprises two output lines.

Refer to the rejection of the parent claim(s) and claim 7.

Regarding **claim 49**, *Nam* in view of *Decker* in further view of *Fossum* discloses the system of claim 48, wherein said first sample and hold circuits

sample and hold reset and pixel signals associated with the green pixels, the pixel signals being output on one output line of the first output channel and the reset signals being output on a second output line of the first output channel.

Refer to the rejection of the parent claim(s) and claim 7.

Regarding **claim 50**, *Nam* in view of *Decker* in further view of *Fossum* discloses the system of claim 48, wherein said second sample and hold circuits sample and hold reset and pixel signals associated with the red and blue pixels, the pixel signals being output on one output line of the second output channel and the reset signals being output on a second output line of the second output channel.

Refer to the rejection of the parent claim(s) and claim 7.

5. **Claims 61-62** rejected under 35 U.S.C. 103(a) as being unpatentable over

e. *Nam* (US 2004/0135910 A1)

in view of

f. *Bayer* (US 3,971,065).

Regarding **claim 61**, *Nam* in view of *Bayer* discloses the method of claim 58, wherein said step of storing signals associated with a pixel type other than the first pixel type comprises: determining whether a row being read is even (fig. 7); and if it is determined that the row is even, storing a signal received from a first column in the second storage device (fig. 7, [0054-0056]).

Refer to the rejection of the parent claim(s) and claim **67**.

Regarding **claim 67**, *Nam* further discloses the method of claim 63, wherein said step of storing signals associated with the pixels comprises: determining whether a row being read is even; and if it is determined that the row is even, storing a signal received from a first column in the second storage device.

Nam does not expressly disclose the pixels are red and blue.

Bayer discloses a pattern wherein the pixels are red and blue (fig. 6, col. 5 line 52-col. 6 line 6). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use *Bayer*'s color filter pattern in place of the previous similar pattern (and also reversing the names of the first and second storage devices) because they are functionally equivalent.

Refer to the rejection of the parent claim(s).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Guidash (US 2005/0012836 A1) teaches like pixel types in neighboring columns are held and sampled by the same circuit using a multiplexer.

Fossum (US 5,841,126 A, Fossum et al.) teaches an output channel with two output lines for signal and reset levels.

Borg (US 6,476,864 B1, Borg et al.) teaches an output channel with two output lines for signal and dummy levels.

Hagihara (US 6,822,211 B2) teaches an output channel with two output lines for signal and reset levels.

Misawa (US 7,218,348 B2) teaches red and blue pixels in adjacent columns on the same row.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Saunders whose telephone number is 571.270.3319. The examiner can normally be reached on Mon-Thur 8:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on 571.272.7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/PS/

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